AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A system comprising:

trigger-matching logic to capture an incoming read/write request cycle from ~~an upstream~~ a requesting device and to determine if the captured incoming read/write request cycle matches at least one trigger condition of one or more of trigger conditions; and

control logic coupled to the trigger-matching logic to select ~~a set of~~at least one single instruction~~s~~ upon detection of the at least one matched trigger condition and to execute one or more operations ~~as~~ specified by the selected ~~set of~~single instruction~~s~~ to modify the captured incoming read/write request cycle prior to transmission to a ~~downstream destination~~designated end device, wherein the ~~set of~~at least one single instruction~~s~~ is selected based on the at least one matched trigger condition and the ~~upstream~~ requesting device is different from the ~~downstream destination~~designated end device.

2. (Original) The system of claim 1, wherein the trigger-matching logic and the control logic are incorporated within an Input/Output (I/O) chip.

3. (Currently Amended) The system of claim 1, wherein the control logic can execute an operation which involves logically combining a selected operand entry with a selected register containing information from the captured cycle in response to the selected single instruction.

4. (Currently Amended) The system of claim 2, wherein the control logic can execute an operation which causes a new cycle to be created and forwarded to a downstream bus of the I/O controller in response to the selected single instruction.

5. (Currently Amended) The system of claim 1, wherein the control logic can execute an operation which involves modifying the captured incoming read/write request cycle in response to the selected single instruction.

6. (Currently Amended) The system of claim 1, wherein the control logic can execute an operation which causes a timed delay or a conditional delay to be inserted in response to the selected single instruction.

7. (Currently Amended) A method comprising:

capturing an incoming read/write request cycle from ~~an upstream~~a requesting device;

loading information from the captured read/write request cycle into a first register;

comparing the information stored in the first register with one or more trigger conditions;

selecting ~~a sequence of~~at least one single instructions based on a matched trigger condition; and

executing the selected single instructions ~~sequentially~~ to modify the captured incoming read/write request cycle prior to transmission to ~~a downstream destination~~ designated end-device, wherein the ~~upstream~~ requesting device is different from the ~~downstream destination~~ designated end-device.

8. (Previously Presented) The method of claim 7, wherein the incoming read/write request cycle is received within an I/O controller chip.

9. (Currently Amended) The method of claim 7, wherein executing of the single instructions comprises:

logically combining a selected operand entry with a selected register containing information captured from the received read/write request cycle.

10. (Currently Amended) The method of claim 8, wherein executing the single instructions comprises:

generating a new read/write request cycle and forwarding the new read/write request cycle to a downstream bus of the I/O controller chip.

11. (Currently Amended) The method of claim 7, wherein executing the single instructions comprises:

modifying a cycle type section of the incoming read/write request cycle.

12. (Currently Amended) The method of claim 7, wherein executing the single instructions comprises:

modifying an address section of the incoming read/write request cycle.

13. (Currently Amended) The method of claim 7, wherein executing the single instructions comprises:

modifying a data section of the incoming read/write request cycle.

14. (Original) The method of claim 7, wherein executing the instructions comprises:

inserting a timed delay or a conditional delay.

15. (Currently Amended) A patch module comprising:

a cycle capture unit to capture read/write request cycles forwarded by a processor as ~~an upstream~~a requesting device;

a plurality of trigger registers to store trigger conditions;

a trigger comparator coupled between the cycle capture unit and the trigger registers to determine if information associated with the captured read/write request cycle matches at least one trigger condition of the trigger conditions stored in the trigger registers;

an instruction storage to store instructions;

an instruction select unit to select ~~a set of~~at least one single instructions from the instruction storage based on the at least one matched trigger condition;

an instruction execution unit to execute the ~~set of~~single instructions selected by the instruction select unit to modify the captured incoming read/write request cycle prior to transmission to a ~~downstream destination~~ designated end-device, wherein the ~~upstream~~ requesting device is different from the ~~downstream destination~~ designated end-device.

16. (Original) The patch module of claim 15, wherein the patch module is embedded within an I/O controller chip and can be programmed by a user to workaround conditions and defects existing in the I/O controller chip.

17. (Currently Amended) The patch module of claim 15, wherein the instruction execution unit can execute ~~an~~ a single instruction that comprises:

a first field to specify a type of operation to be performed, wherein the type of operations identified by the first field includes (1) timed delay operation, (2) conditional delay operation, (3) generating new cycle operation, and (4) modifying the capture request cycle operation; and

a second field to specify whether or not a cycle generated by the instruction is to be forwarded to downstream bus.

18. (Original) The patch module of claim 15, wherein the instruction execution unit can execute an instruction that comprises:

a third field to select a register to modify;

a fourth field to select an operand entry from an operand array; and

a fifth field to select a logic gate for combining the selected register with the selected operand entry.

19. (Previously Presented) The patch module of claim 17, wherein the captured incoming read/write request cycle is a non-posted cycle.

20. (Previously Presented) The patch module of claim 19, wherein the instruction execution unit can execute an instruction that comprises:

a fifth field to specify whether a completion queue is to be loaded with unmodified header information from the captured non-posted cycle or loaded with modified header information associated with modified request cycle that is generated by the control logic; and

a sixth field to specify whether or not a completion associated with the captured read/write request cycle is to be discarded.

21. (Currently Amended) A machine-readable medium that provides instructions, which when executed by a processor cause the processor the perform operations comprising:

capturing an incoming read/write request cycle from ~~an upstream~~a requesting device;

comparing information obtained from the captured incoming read/write request cycle to one or more trigger conditions;

generating ~~a sequence of~~at least one single instructions to be executed in response to a matched trigger condition; and

executing the generated instruction~~s sequentially~~ to modify the captured incoming read/write request cycle prior to transmission to a ~~downstream destination~~ designated end-device, wherein the ~~upstream~~ requesting device is different from the ~~downstream destination~~ designated end-device.

22. (Currently Amended) The machine-readable medium of claim 21, wherein the operations performed by the processor further comprise:

generating a new read/write request cycle and forwarding the new read/write request cycle to a downstream bus of an I/O controller chip in response to the generated single instruction.

23. (Currently Amended) The machine-readable medium of claim 21, wherein the operations performed by the processor further comprise:

modifying a cycle type section of the incoming read/write request cycle in response to the generated single instruction.

24. (Currently Amended) The machine-readable medium of claim 21, wherein the operations performed by the processor further comprise:

modifying an address section of the incoming read/write request cycle in response to the generated single instruction.

25. (Currently Amended) The machine-readable medium of claim 21, wherein the operations performed by the processor further comprise:

modifying a data section of the incoming read/write request cycle in response to the generated single instruction.

26. (Currently Amended) The machine-readable medium of claim 21, wherein the operations performed by the processor further comprise:

inserting a timed delay or a conditional delay in response to the generated single instruction.